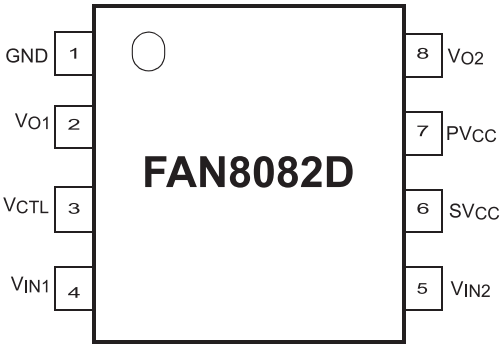
7. IC Block Diagrams

7-1 Main

7-1-1. FAN8082D

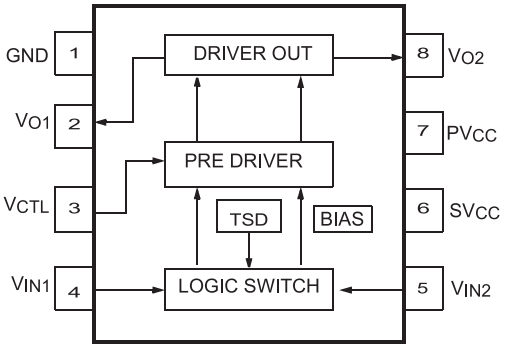
Pin Assignments



Pin Definitions

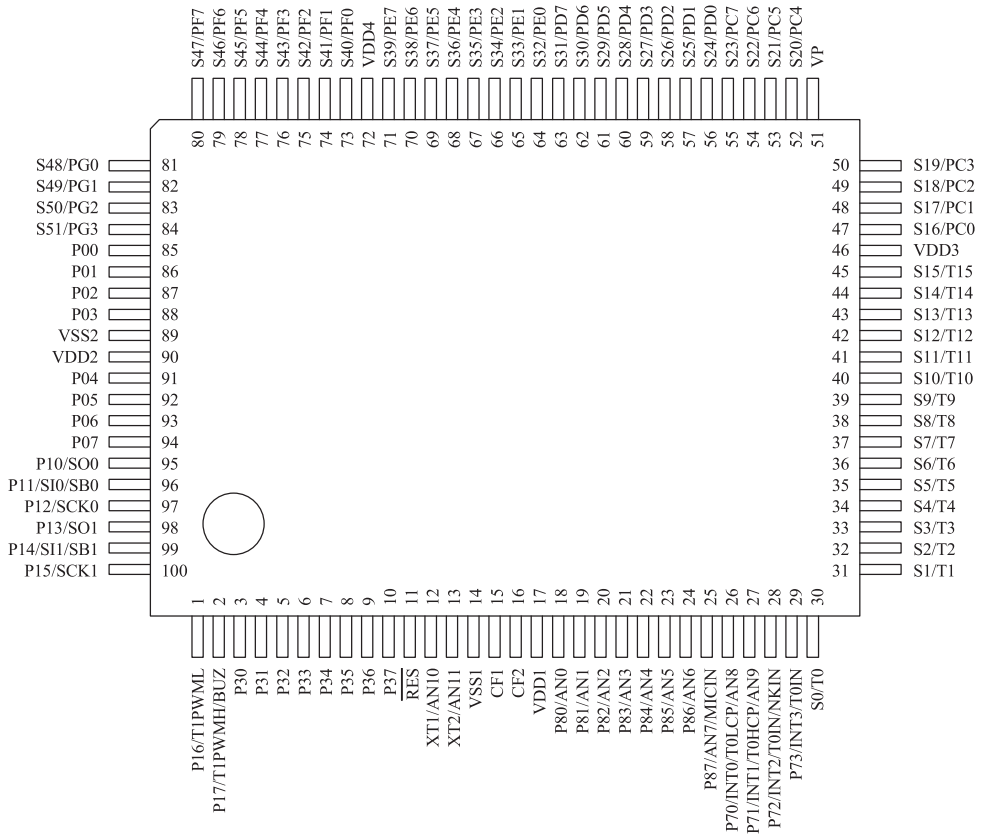
Pin Number	Pin Name	I/O	Pin Function Description
1	GND	-	Ground
2	V_{O1}	O	Output 1
3	V_{CTL}	I	Motor speed control
4	V_{IN1}	I	Input 1
5	V_{IN2}	I	Input 2
6	SV_{CC}	-	Supply voltage (Signal)
7	PV_{CC}	-	Supply voltage (Power)
8	V_{O2}	O	Output 2

Internal Block Diagram



LC87F66C8A

Pin Assignment

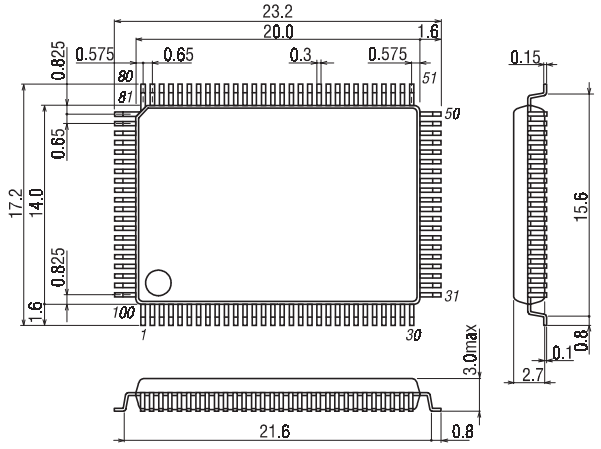


SANYO: QIP-100E

Package Dimensoin

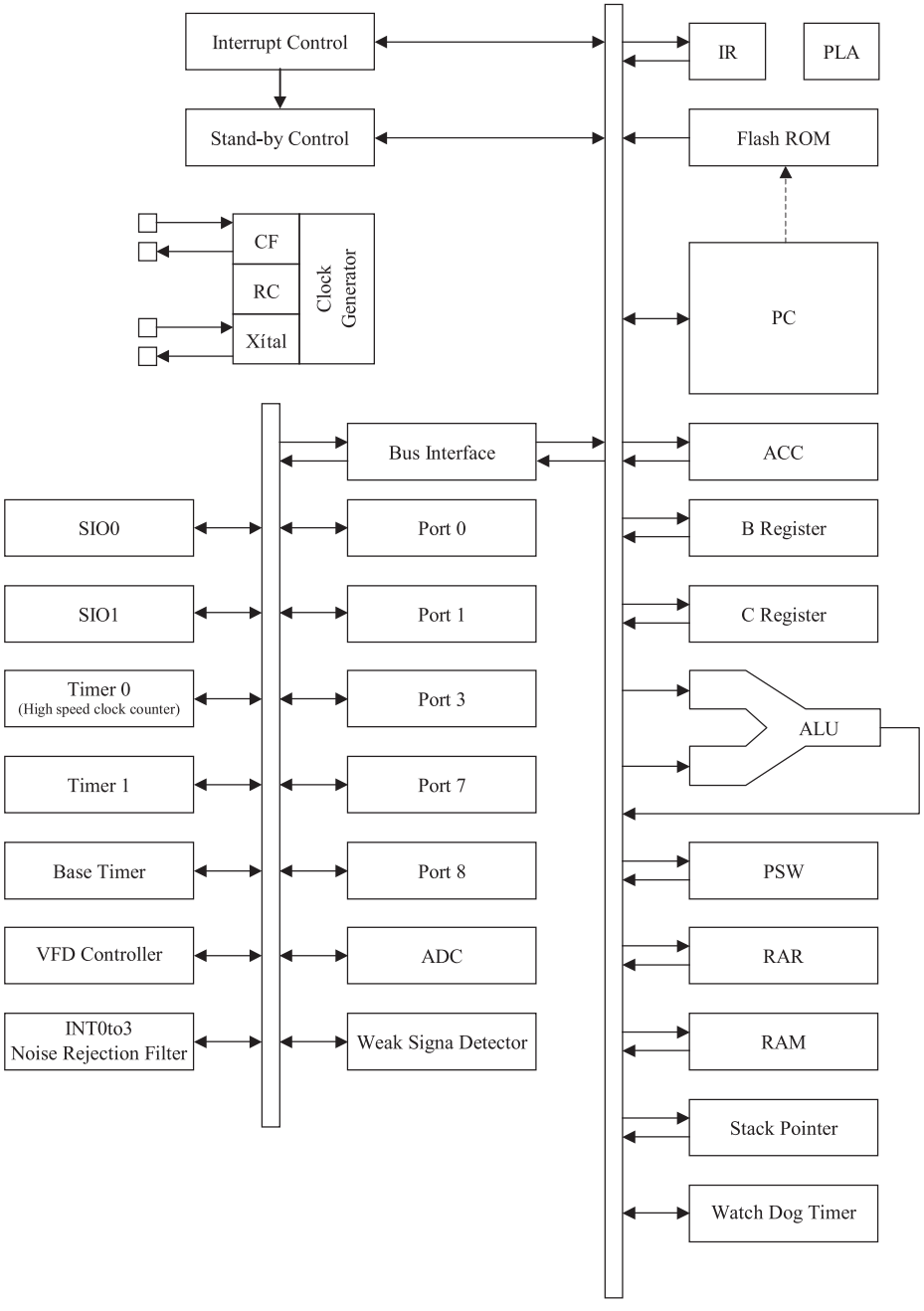
(unit : mm)

3151



SANYO: QIP-100E

System Block Diagram



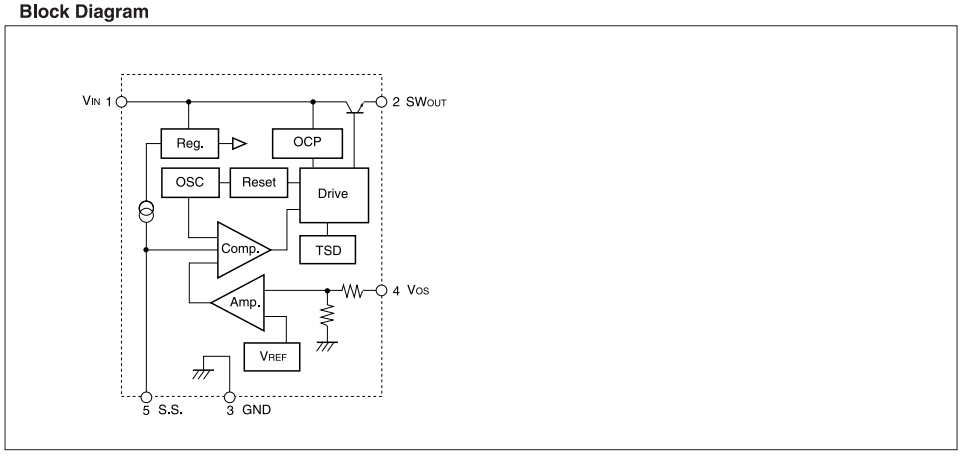
Pin Assignment

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>VSS1
VSS2</td><td>-</td><td>□Power supply (-)</td><td>No</td></tr>
<tr><td>VDD1
VDD2
VDD3
VDD4</td><td>-</td><td>□Power supply (+)</td><td>No</td></tr>
<tr><td>VP</td><td>-</td><td>□Power supply (-)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>□8bit input/output port
□data direction programmable in nibble units
□Use of pull-up resistor can be specified in nibble units
□Input for HOLD release
□Input for port 0 interrupt
□15V withstand at N-channel open drain output</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>□8bit input/output port
□data direction programmable for each bit
□Use of pull-up resistor can be specified for each bit
□Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>PORT3
P30 to P33</td><td>I/O</td><td>□8bit Input/output port
□Data direction can be specified for each bit
□Use of pull-up resistor can be specified for each bit
□15V withstand at N-channel open drain output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>□4bit Input/output port
□Data direction can be specified for each bit
□Use of pull-up resistor can be specified for each bit
□Other functions
P70: INT0 input/HOLD release input/Timer0L capture Input/output for watchdog timer
P71: INT1 input/HOLD release input/Timer0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/Timer0L capture input/High speed clock counter input
P73: INT3 input(noise rejection filter attached input)/timer 0 event input/Timer 0H capture input
AD input port: AN8(P70), AN9(P71)
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
</table>

Pin name	I/O	Function description	Option
PORT8 P80 to P87	I/O	□8bit Input/output port □Input/output can be specified in a bit unit □Other functions: AD input port: AN0 to AN7 Weak signal detector input port: MICIN(P87)	No
S0/T0 to S8/T8	O	□Large current output for VFD display controller digit (can be used for segment)	No
S9/T9 to S15/T15	O	□Large current output for VFD display controller segment/digit	No
S16 to S23	I/O	□Output for VFD display controller segment/digit □Other functions: High voltage input port: PC0 to PC7	No
S24 to S31	I/O	□Output for VFD display controller segment □Other functions: High voltage input port: PD0 to PD7	No
S32 to S39	I/O	□Output for VFD display controller segment □Other functions High voltage input port: PE0 to PE7	No
S40 to S47	I/O	□Output for VFD display controller segment □Other functions: High voltage input/output port: PF0 to PF7	No
S48 to S51	I/O	□Output for VFD display controller segment □Other functions: High voltage input/output port: PG0 to PG3	No
$\overline{\text{RES}}$	I	Reset terminal	No
XT1	I	□Input for 32.768kHz crystal oscillation □Other functions: General purpose input port When not in use, connect to VDD1. AD input port: AN10	No
XT2	I/O	□Output for 32.768kHz crystal oscillation □Other functions: General purpose input port When not in use, set to oscillation mode and leave open circuit. AD input port: AN11	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

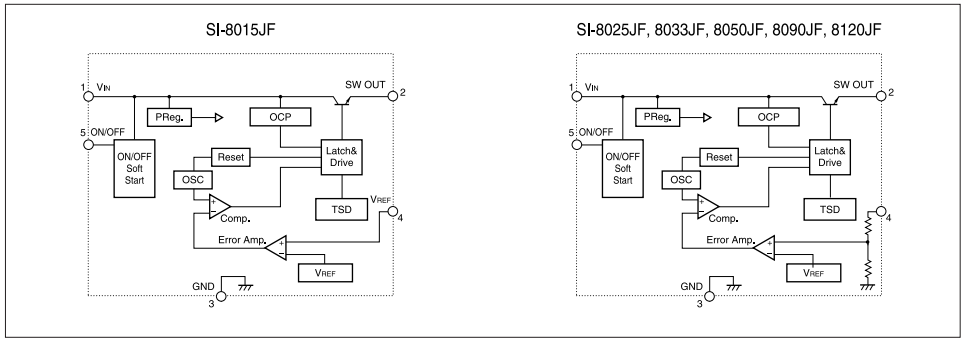
7-1-3. SI-8050SE

Block Diagram



7-1-4. SI-8090JFE

Block Diagram



Block Diagram

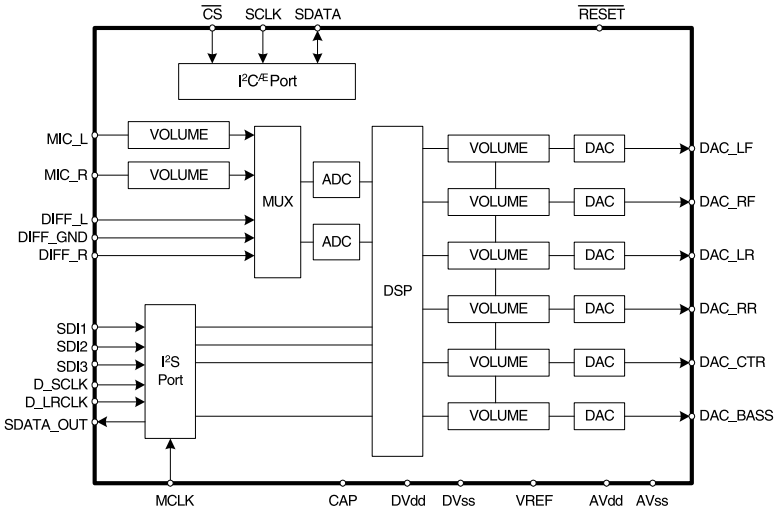
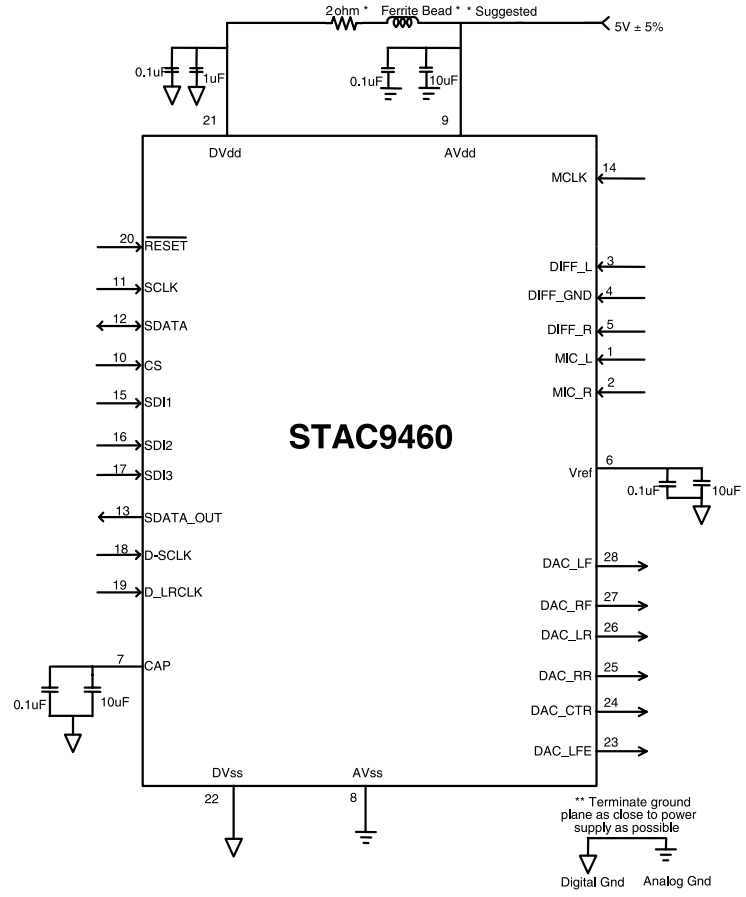
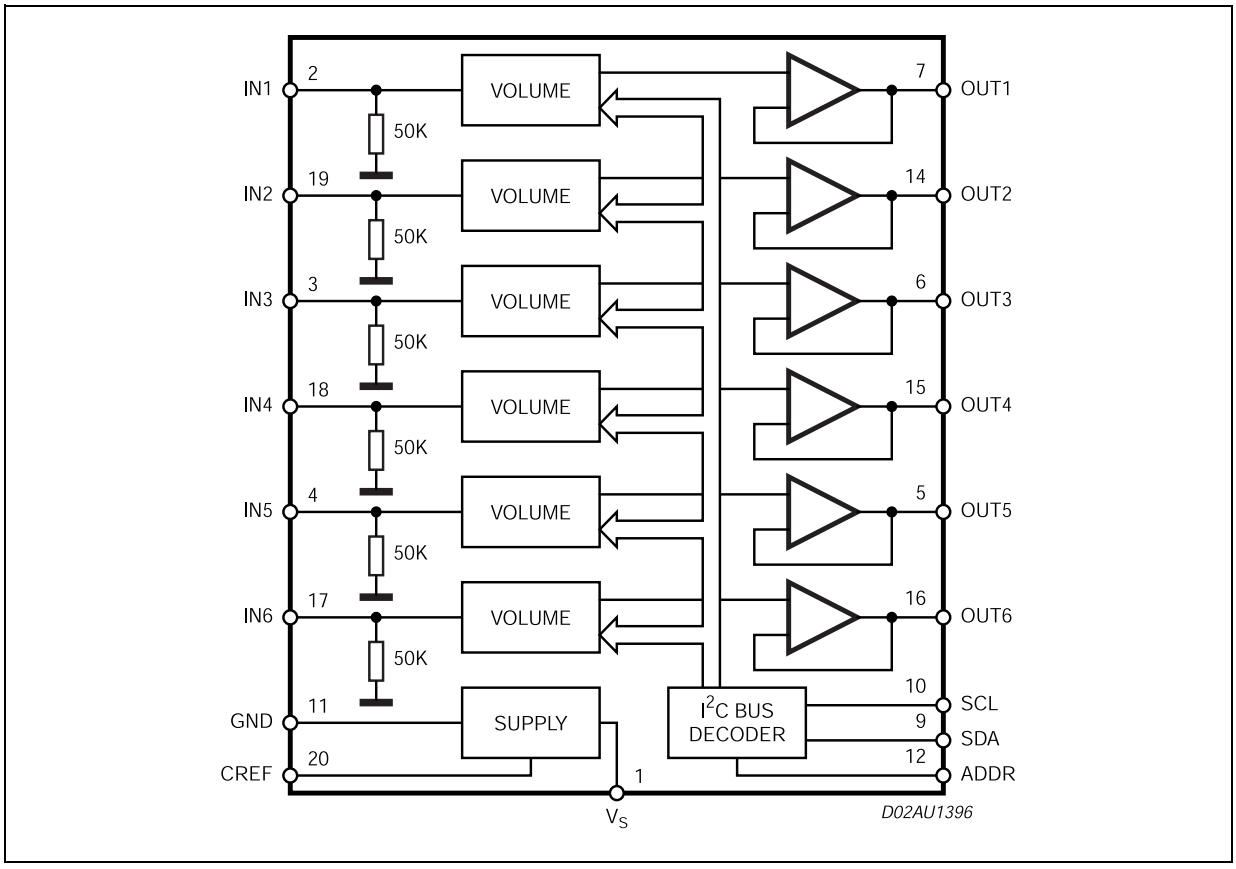


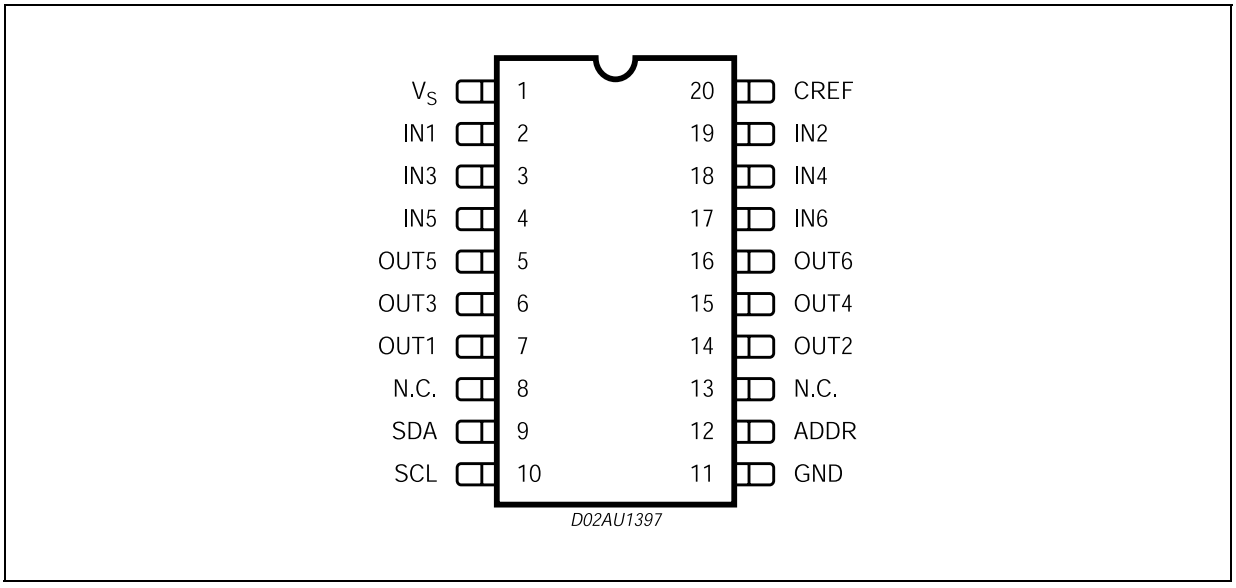
Figure 1. STAC9460 Block Diagram



BLOCK DIAGRAM

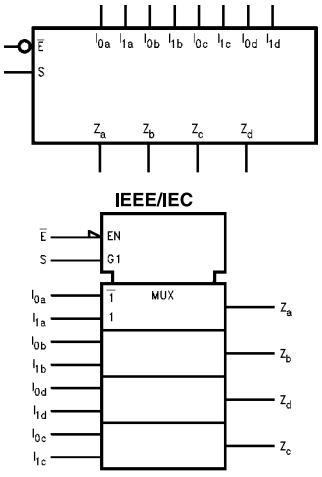


PIN CONNECTION

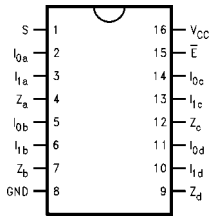


7-1-7. 74VHC157

Logic Symbols



Connection Diagram

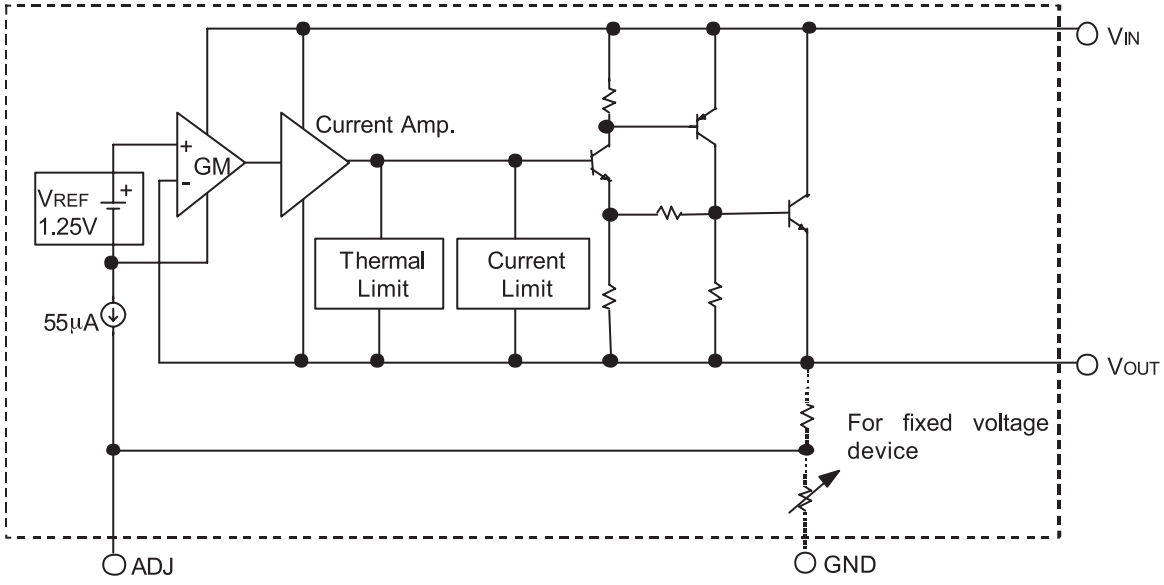


Pin Descriptions

Pin Names	Description
I_{0a}ñI_{0d}	Source 0 Data Inputs
I_{1a}ñI_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_añZ_d	Outputs

7-1-8. AIC1117A

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

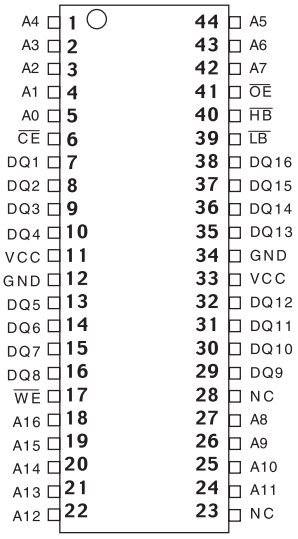
ADJ PIN - Providing V_{REF}=1.25V (typ.) for adjustable V_{OUT}. $V_{REF}=V_{OUT}-V_{ADJ}$ and I_{ADJ}=55μA (typ.)
(GND PIN - Power ground.)

VOUT PIN - Adjustable output voltage.

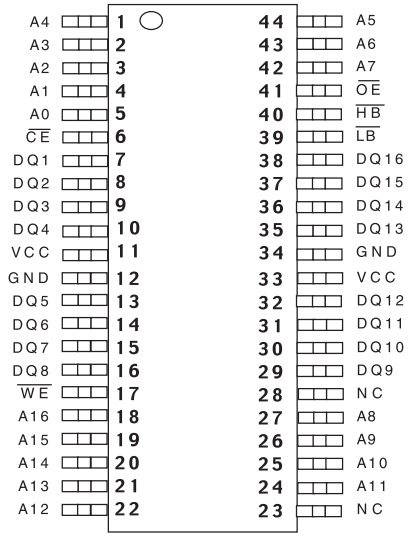
VIN PIN - Power Input.

PIN ASSIGNMENT

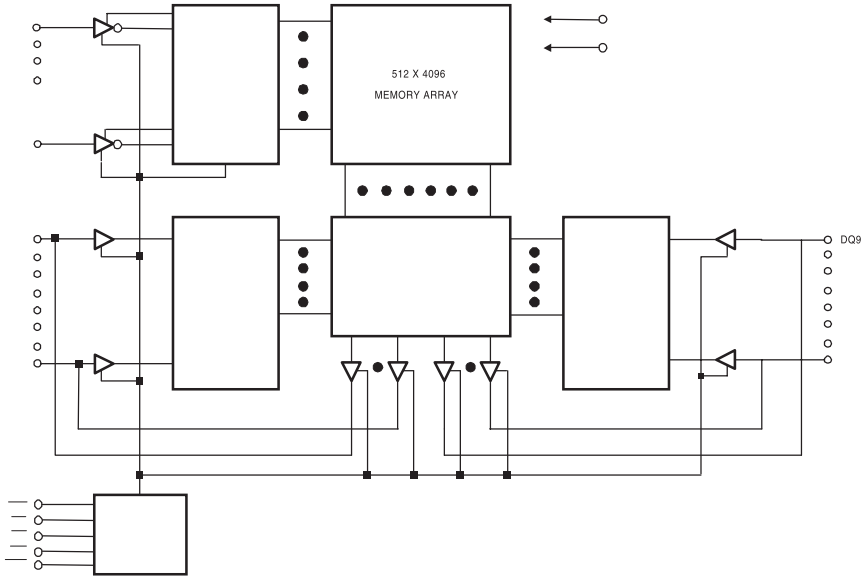
SOJ Top View



TSOP (TypeII) Top View



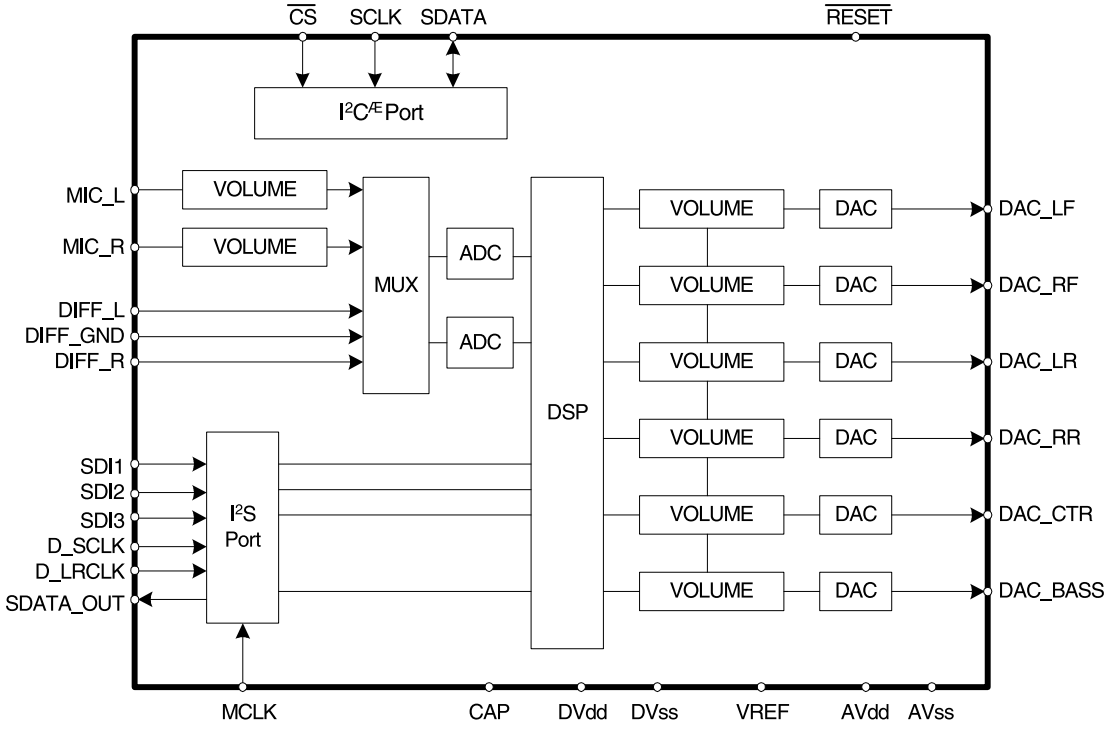
Block Diagram



Pin Descriptions

Pin No.	Symbol	Description
1 - 5, 18 - 22, 24-27, 42 - 44	A0 - A16	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	DQ1 - DQ16	Data Inputs/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Lower Byte Enable Input (DQ1 to DQ8)
40	$\overline{HB}$	Higher Byte Enable Input (DQ9 to DQ16)
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
23, 28	NC	No Connection

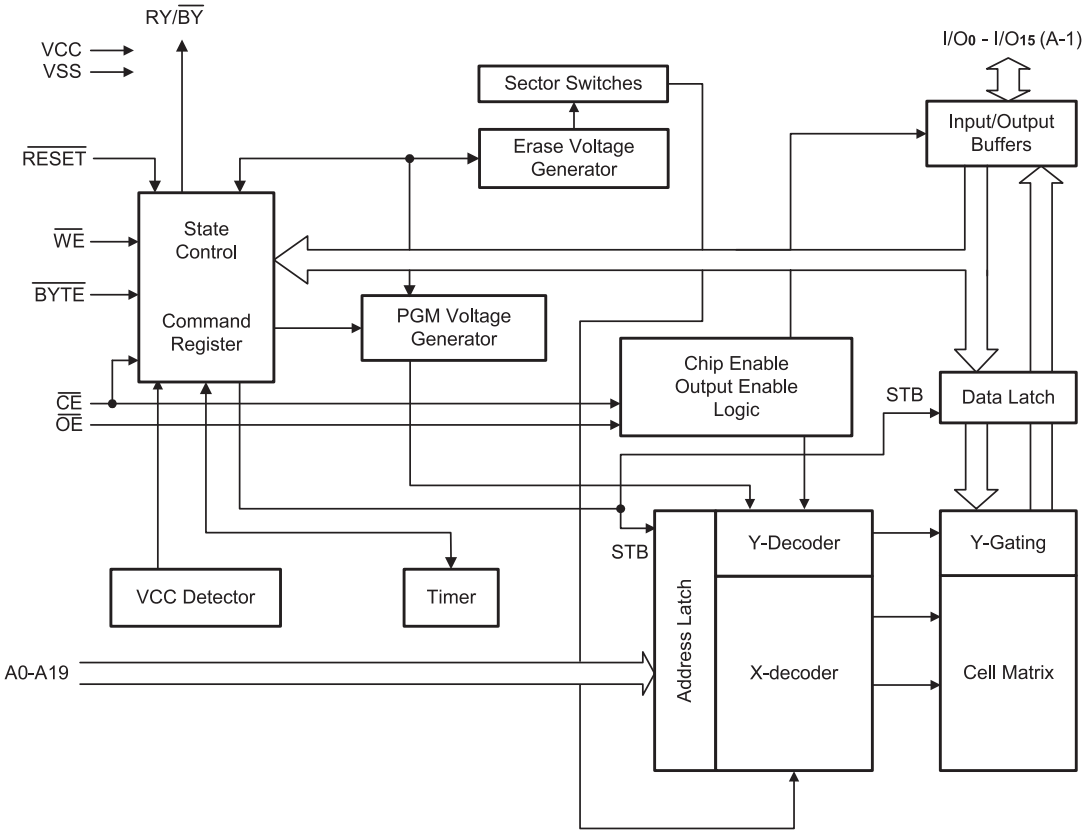
7-1-10. STAC9460



7-2 DVD

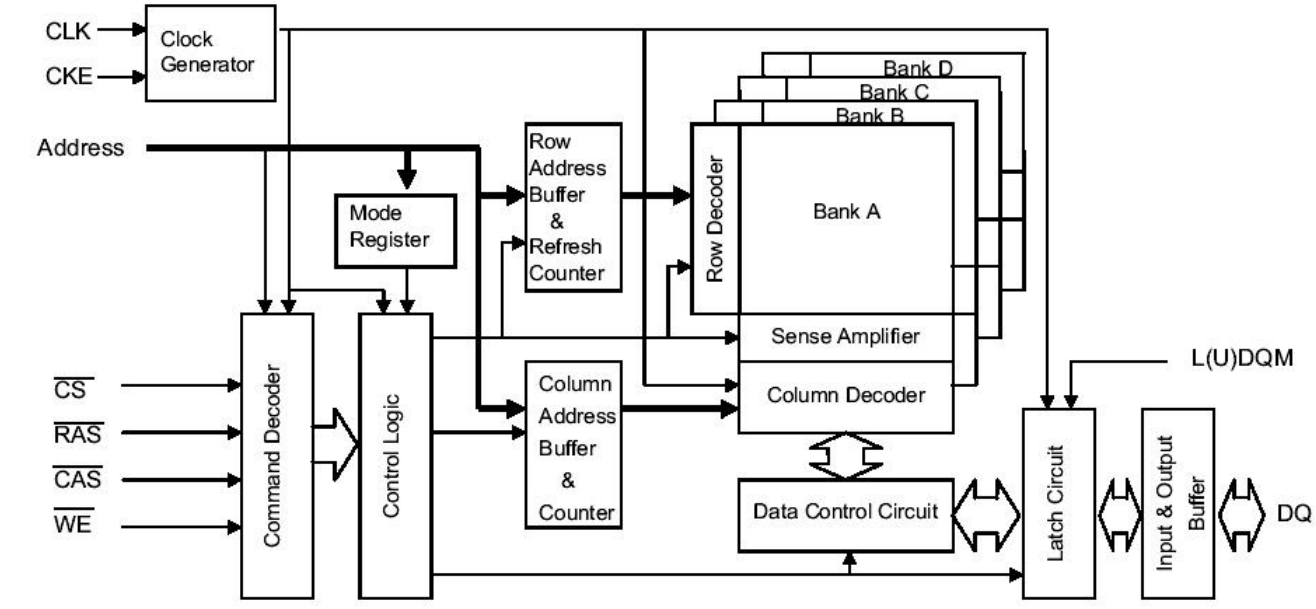
7-2-1. A29L160

Block Diagram

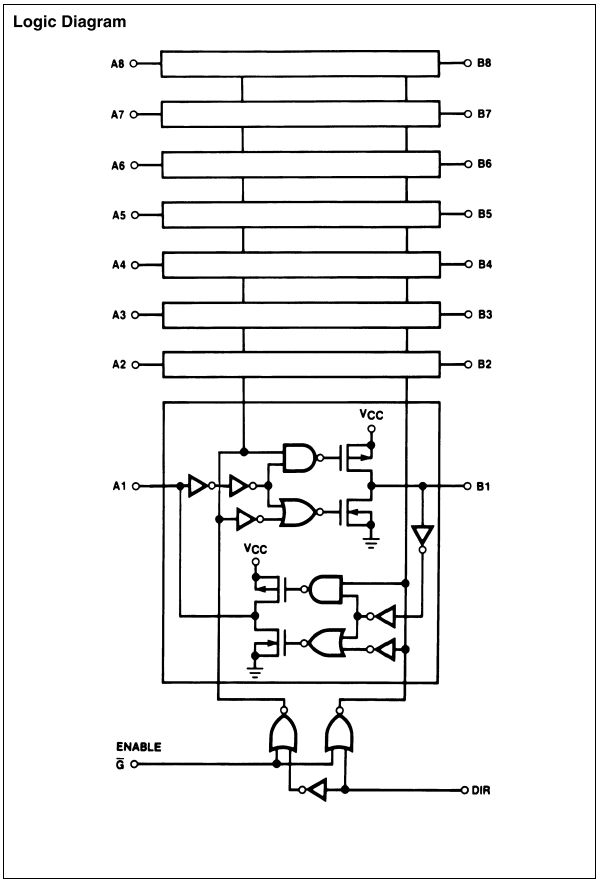


7-2-2. ESMT_M12L128168A

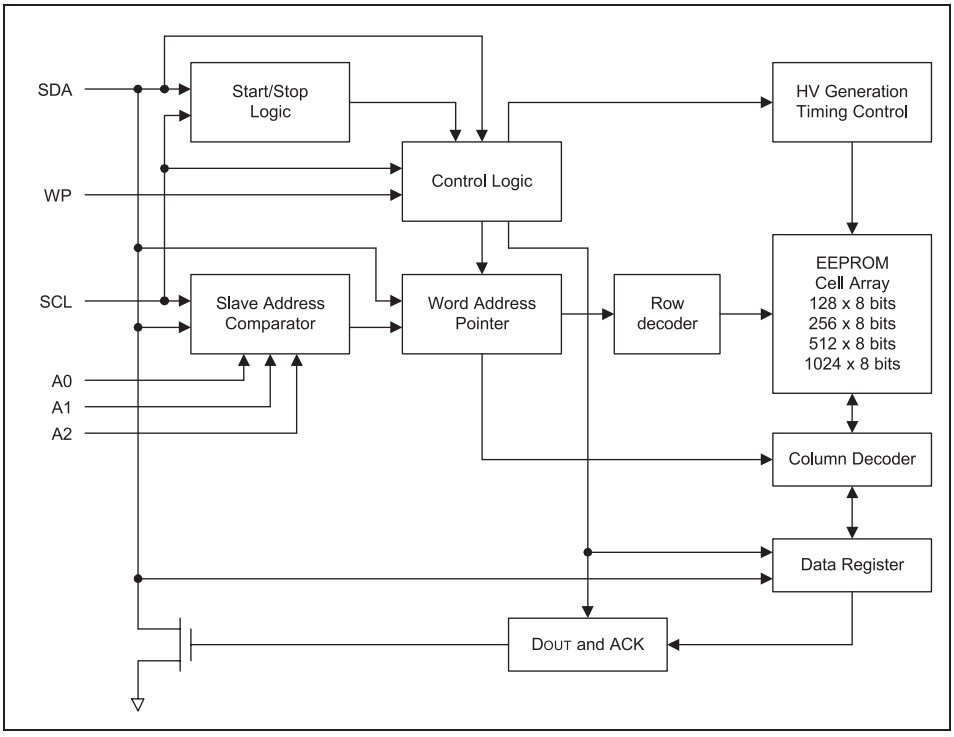
BLOCK DIAGRAM



7-2-3. 74HCT245



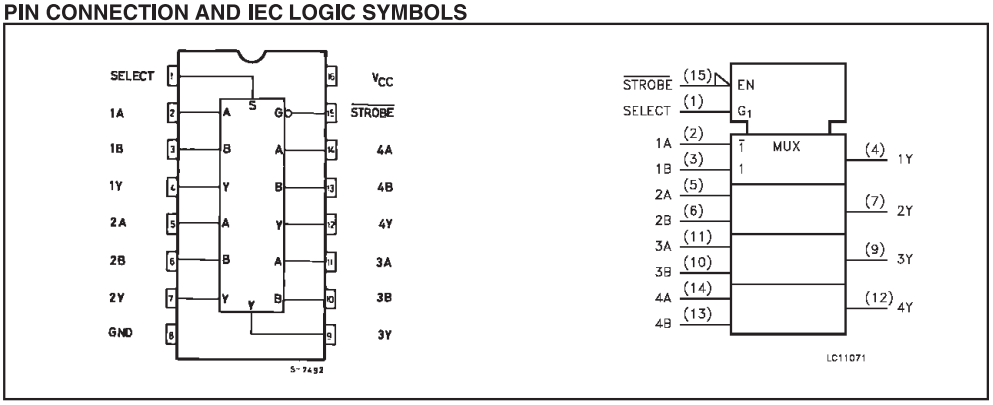
7-2-4. S524C20D21_20D41



S524C20D11/20D21/80D41/80D81 Block Diagram

7-2-5. STM_74LCX157

PIN CONNECTION AND IEC LOGIC SYMBOLS

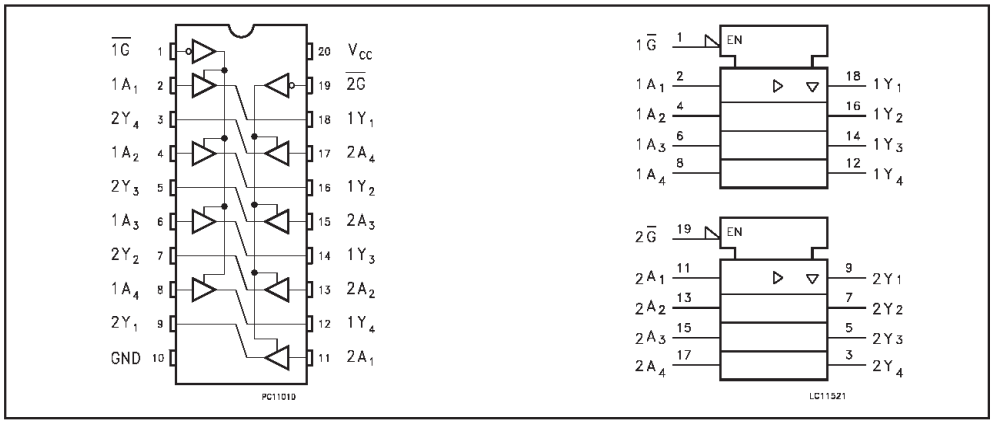


PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Outputs
15	STROBE	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

7-2-6. STM_74LCX244

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

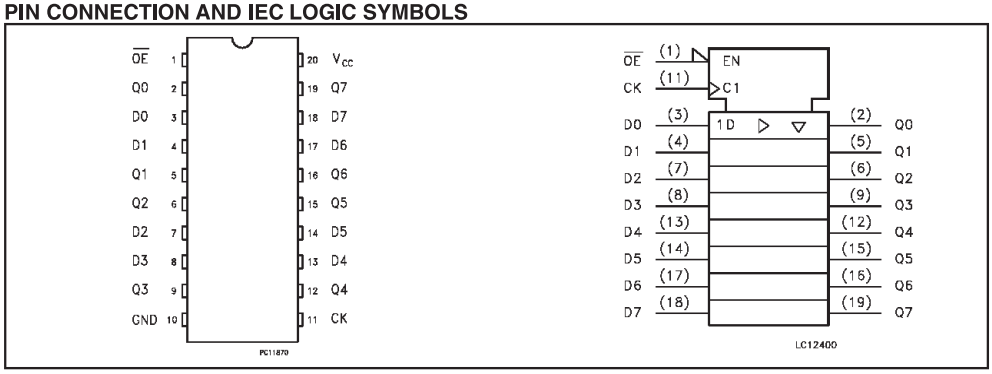
TRUTH TABLE

INPUT		OUTPUT
$\overline{G}$	An	Yn
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

7-2-7. STM_74LCX374

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	OE	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance

DS100 MICOM PORT ASSIGNMENT (LC877448) REV0

(ANYNET,WIRELESS적용)

2003.9.15 ST PARK

NO	PORT	NAME	I/O	TYPE	FUNCTION	NO	PORT	NAME	I/O	TYPE	FUNCTION
1	P06		O			51	PC5	OPT6	I		OPTION
2	P07	DO1	O		CE(LC72131)	52	PC6	OPT7	I		OPTION
3	P10					53	PC7	OPT8	I		OPTION
4	P11	TDI	I		DO(LC72131)	54	VDD2	VDD2			VDD 5V
5	P12	P-ACK	I		PACK ACK	55	VSS2	VSS2			GND
6	P13	UWATT1	O		UWATT1	56	PD0	OPT9	I		OPTION
7	P14	UWATT2	O		UWATT2	57	PD1	OPT10	I		OPTION
8	P15	I/O SEL	O		ANY-NET	58	PD2	OPT11	I		OPTION
9	P16	CK1	O		FUN/VFD/TU/CODEC CLK	59	PD3	OPT12	I		OPTION
10	P17	DO1	I/O		FUN/VFD/TU/CODEC DATA	60	PD4	OPT13	I		OPTION
11	RES	RESET	I		MICOM RESET	61	PD5	OPT14	I		OPTION
12	XT1	XT1	I		NC	62	PD6	OPT15	I		OPTION
13	XT2	XT2	O		NC	63	PD7	OPT16	I		OPTION
14	VSS1	GND			GND	64	PE0	P-TXD	O		P-TXD
15	CF1	CF1	I		10MHZ OSC IN	65	PE1	P-STB	O		P-STB (Pack Input)
16	CF2	CF2	O		10MHZ OSC OUT	66	PE2	P-SENS	I		POWER SENSE
17	VDD1	VDD1			VDD 5V	67	PE3		I		
18	P80	AD1	I	AD	KEY A/D 1	68	PE4		I		
19	P81	PRO	I	AD	PROTECTION(Active H)	69	PE5		I		
20	P82	ST	I	AD	STEREO	70	PE6		O		
21	P83	TUNED	I	AD	TUNED	71	PE7		O		
22	P84	H-SEN	I	AD	HP SENSE	72	PF0		O		
23	P85	M-SEN	I	AD	MIC SENSE	73	PF1		O		
24	P86	RDS-IN	I	AD	RDS DATA IN	74	PF2				
25	P87			AD		75	PF3				
26	P70	BREQ	I	INT	RDS CLK	76	PF4				
27	P71	P-RXD	I	INT	PACK RXD (Pack Output)	77	PF5	VR-LED	O		VOLUME LED
28	P72			INT		78	PF6				
29	P73	REMO	I	INT	REMOCON IN	79	PF7	BLK	O		BLK(VFD)
30	PA0	SCART-M	O		SCART MUTE	80	PL6	EVR IN	I		VOLUME UP
31	PA1	V-SW1	O		A/V SW1	81	PL5	EVR IN	I		VOLUME DOWN
32	PA2	V-SW2	O		A/V SW2	82	PL4				
33	PA3	AV1	O		V-CTRL1	83	PL0				
34	PA4	AV2	O		V-CTRL2	84	PL1				
35	PA5					85	PL2				
36	PA6	ECHO1	O		ECHO LEVEL1	86	PL3				
37	PA7	ECHO2	O		ECHO LEVEL2	87	P30				
38	PB0	F/W-M	O		FRONT-SUB MUTE	88	P31				
39	PB1	C-M	O		CENTER MUTE	89	VSS3	VSS3			GND
40	PB2	R-M	O		REAR MUTE	90	VDD3	VDD3			VDD 5V
41	PB3	WRST1	O		WIRERESS RESET1	91	P32				
42	PB4	WRST2	O		WIRERESS RESET2	92	P33				
43	PB5		O			93	P34	VR-CLK	O		TDA7448 CLK
44	PB6	COD	O		CODEC RESET	94	P35	VR-DO	O		TDA7448 DO
45	PB7		O			95	P00	P-ON	O		POWER ON
46	PC0	OPT1	I		OPTION	96	P01	VFD-CE	O		CE1
47	PC1	OPT2	I		OPTION	97	P02	F/W-M	O		FRONT-SUB MUTE
48	PC2	OPT3	I		OPTION	98	P03	C-M	O		CENTER MUTE
49	PC3	OPT4	I		OPTION	99	P04	R-M	O		REAR MUTE
50	PC4	OPT5	I		OPTION	100	P05	AMP	O		AMP ON

<UPDATE CONNECTION>

6	5	CLK
5	4	DATA0
4	3	DATA1
3	17	VDD
2	14	GND
1	11	RESET

<PACK CONNECTION>

DVD-PACK		MICOM
P-RXD	<--	P-TXD
P-TXD	-->	P-RXD
P-ACK	<--	P-STB
P-STB	-->	P-ACK